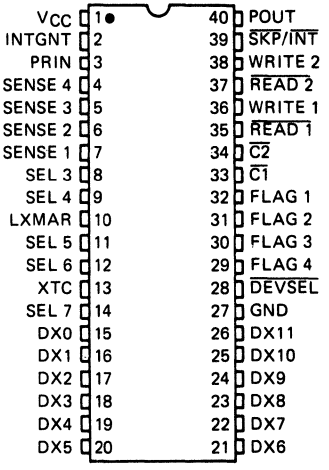
HARRIS

HD-6101
CMOS PARALLEL INTERFACE ELEMENT (PIE)

Features

- HM-6100 COMPATIBLE
- LOW POWER STANDBY -500μW MAX
- SINGLE SUPPLY 4–11 VOLTS
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- 4 PROGRAMMABLE OUTPUTS (FLAGS)
- 4 PROGRAMMABLE SENSE INPUTS
- CONTROL FOR TWO 12 BIT INPUT PORTS
- CONTROL FOR TWO 12 BIT OUTPUT PORTS
- PRIORITY VECTORED INTERRUPTS
- UP TO 31 PIE'S PER SYSTEM
- 16 INSTRUCTIONS FOR PIE CONTROL

Pinout

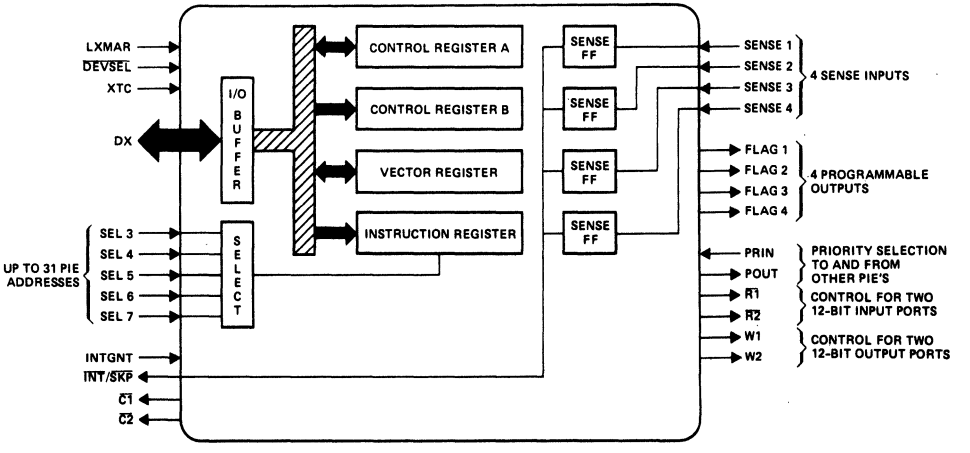


Description

The HD-6101 Parallel Interface Elements (PIE) are high speed, low power, silicon gate CMOS general purpose devices which provide addressing interrupt and control for a variety of peripheral functions, such as UARTs, FIFOs, Keyboards, etc. Data transfers between the HM-6100 CMOS Microprocessor and the HD-6101 are via Input-Output Transfer (IOT) instructions, control lines and DX bus.

Data transfers between peripheral devices and the DX bus are controlled by the PIE via 2 read, 2 write, 4 sense and 4 flag functions. Internal PIE registers are programmed under software control for write polarities, sense levels or edges, flag values and interrupt enables. Another software controlled register stores the address for vectored interrupt operation.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC + 0.3V)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101-9	-40°C to +85°C
Military HD-6101-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		+1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
V_{OH}	Logical "1" Output Voltage(1)	2.4			V	I_{OH} = -0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage	-1.0		+1.0	μA	$0V \leqslant V_O \leqslant V_{CC}$
I_{CC}	Supply Current (Static)		1.0	100	μA	$V_{IN} = V_{CC}$, Freq. = 0
C_I	Input Capacitance(2)		5	7	pF	
C_O	Output Capacitance(2)		8	10	pF	
C_{IO}	Input/Output Capacitance(2)		8	10	pF	

NOTE: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		T_A = 25°C V_{CC} = 5.0V(1)		T_A = INDUSTRIAL V_{CC} = 5V ±10%		T_A = MILITARY V_{CC} = 5V ±10%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
tDR	Delay: $\overline{DEVSEL}$ to $\overline{READ}$		200		300		330	ns	C_L = 50pF
tDW	Delay: $\overline{DEVSEL}$ to WRITE	100	220	140	300	150	330	ns	See Timing
tDF	Delay: $\overline{DEVSEL}$ to FLAG		200		375		415	ns	Diagram
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$		160		460		510	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		210		460		510	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		350		460		510	ns	
tLX	LXMAR Pulse Width	200		240		265		ns	
tAS	Address Set-Up Time	60		80		90		ns	
tAH	Address Hold Time	100		125		140		ns	
tDS	Data Set-Up Time	50		80		80		ns	
tDH	Data Hold Time	100		100		110		ns	

NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC +0.3V)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5%; T_A = Industrial

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			.8	V	
	I_{IL}	Input Leakage	-10		+10	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
	V_{OH}	Logical "1" Output Voltage(1)	2.4			V	I_{OH} = -0.2mA
	V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 1.6mA
	I_O	Output Leakage	-10		+10	μA	$0V \leqslant V_O \leqslant V_{CC}$
	I_{CC}	Supply Current (Static)		1.0	800	μA	$V_{IN} = V_{CC}$, Freq. = 0
	C_I	Input Capacitance(2)		5	7	pF	
	C_O	Output Capacitance(2)		8	10	pF	
	C_{IO}	Input/Output Capacitance(2)		8	10	pF	

NOTES: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

			T_A = 25°C V_{CC} = 5.0V(1)		T_A = INDUSTRIAL V_{CC} = 5V ±5%			
	SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
A.C.	tDR	Delay: $\overline{DEVSEL}$ to $\overline{READ}$		230		375	ns	C_L = 50pF
	tDW	Delay: $\overline{DEVSEL}$ to WRITE	100	240	125	375	ns	See Timing
	tDF	Delay: $\overline{DEVSEL}$ to FLAG		230		475	ns	Diagram
	tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$		190		560	ns	
	tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP/INT}$		250		560	ns	
	tDA	Delay: $\overline{DEVSEL}$ to DX		400		560	ns	
	tLX	LXMAR Pulse Width	230		300		ns	
	tAS	Address Set-Up Time	80		100		ns	
	tAH	Address Hold Time	120		150		ns	
	tDS	Data Set-Up Time	60		90		ns	
	tDH	Data Hold Time	120		150		ns	

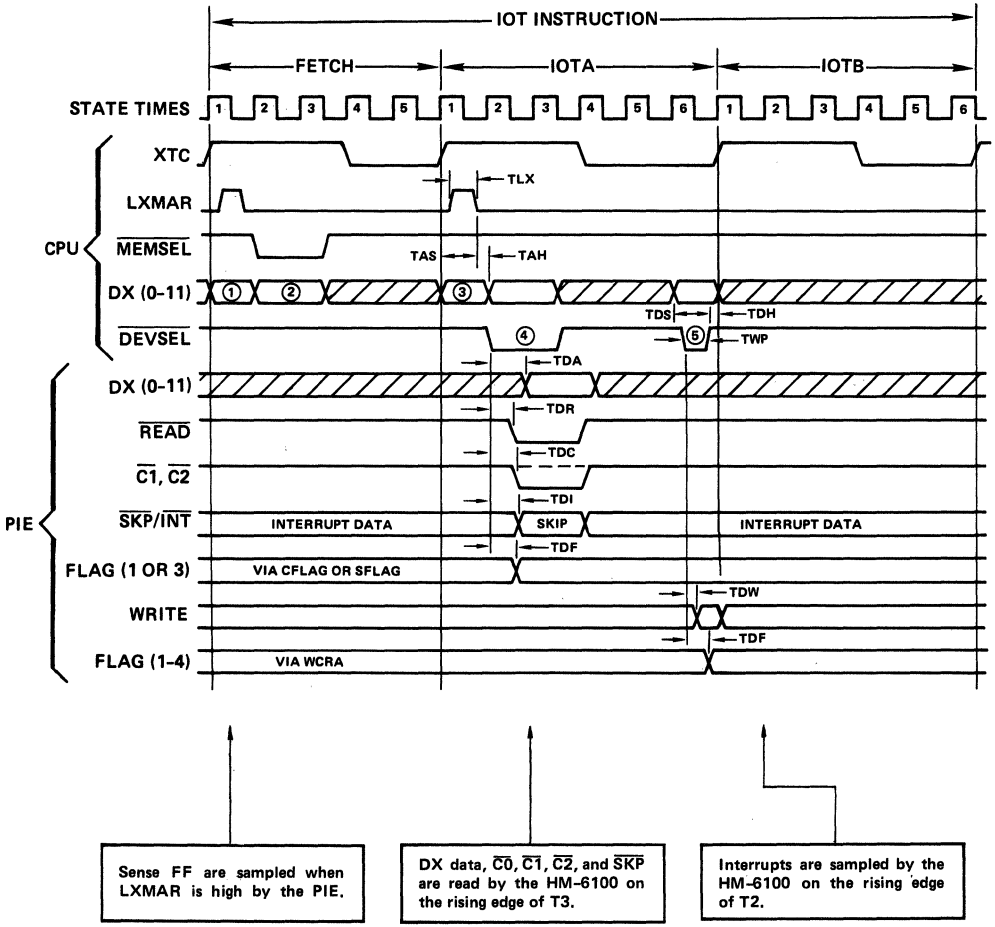
NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

Timing Diagram

Timing for a typical transfer is shown below. During an instruction fetch the processor places the contents of the PC on the bus (1) and obtains from memory an IOT instruction of the form 6XXX (2). During IOTA of the execute phase the processor places that instruction back on the DX lines (3) and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is high (4) is used by the addressed PIE along with the decoded control information to generate CPU control signals $\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{SKP}}$. Also at this time either the Control Register A or the Interrupt Vector Register are outputed on the DX lines, or control outputs $\overline{\text{READ1}}$ and $\overline{\text{READ2}}$ are generated to gate peripheral data to the DX lines. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is low (5) is used to generate WRITE 1 and WRITE 2 controls. These signals are used to latch accumulator data into peripheral devices.

All PIE timing is generated from HM-6100 signals LXMAR, $\overline{\text{DEVSEL}}$, and XTC. No additional timing signals, clocks, or one shots are required.

Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the HM-6100.

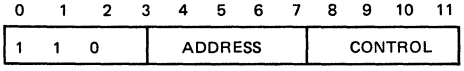


Pie Address and Instructions

The HM-6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the pin programmable select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIEs. Address zero is reserved for IOT's internal to the HM-6100. The four control bits are decoded by the PIE to select one of 16 instructions which are described below.

PIE INSTRUCTION FORMAT



CONTROL	MNEMONICS	ACTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate onto the DX bus to be "OR'ed" with the HM-6100 accumulator data. The HM-6100 accumulator is cleared prior to reading peripheral data when $\overline{CO}$ is asserted low.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the HM-6100 accumulator data on the DX lines into peripheral data registers. The HM-6100 AC is cleared after the write operation when the $\overline{CO}$ input is asserted low.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the $\overline{SKP}/\overline{INT}$ output causing the HM-6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE not assert the $\overline{SKP}/\overline{INT}$ output and the HM-6100 will execute the next instruction.
0100	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time 4 to be "OR" transferred to the HM-6100 AC.
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer HM-6100 AC data on the DX lines during time 5 of IOTA into the appropriate register.
0110 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	HM-6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops.

Programmable Outputs

FLAGs (1-4) - The FLAGs are general purpose outputs that can be set and cleared under program control. GLAG1 follows bit FL1 in Control Register A and etc. FLAGs can be changed by loading new data into CRA via the WCRA commands. In addition, FLAG1 and FLAG3 can be set and cleared directly by the commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.

Programmable Sense Inputs

The sense inputs are used to set sense flip flops (SENSE FF) inside the PIE. For each sense input there are two FF's, one for skip and one for interrupt. Conditions for setting each SENSE FF, levels or edges and positive or negative polarities, are set by control bits SL and SP in CRB.

The SENSE FF's are sampled when LXMAR is high. Interrupt requests are generated only when the sense flip flops are set by an edge and interrupts are enabled by writing to control reg A. Sense flip flops are reset on the following conditions.

CONDITION	SENSE FLIP FLOPS	
	SKIP FF	INTERRUPT FF
CAF Instruction (6007₈)	Clears All	Clears All
SKIP Instruction	Clears Corresponding FF	Clears Corresponding FF
Vectored Interrupt	Not Cleared	Clears Highest Priority FF on Selected PIE After Vectoring
Interrupt Disabled (IE = "0")	Not Cleared	Disables Interrupt by Holding Corresponding FF in Reset State

Controls for Input and Output Ports

READ (1-2) – The $\overline{\text{READ}}$ outputs are activated by the read instructions and are used by peripheral devices to get data onto the DX lines for transfer to the HM-6100. Read lines are active low.

WRITE (1-2) – The WRITE outputs are activated by the write instructions and are used by peripheral devices to load HM-6100 AC data from the DX lines into peripheral data registers. Output polarity is controlled by the WRITE POLARITY bits of CRA. A logic one causes pulses to be positive while a logic zero causes pulses to be negative.

I/O CONTROL LINES – There are three I/O control lines from the PIE to the microprocessor – $\overline{C1}$, $\overline{C2}$, and $\overline{INT}/\overline{SKP}$. The type of data transfer, during an IOT instruction, is specified by the PIE's assertion of the $\overline{C1}$ and $\overline{C2}$ control lines as shown below.

Interrupt and skip information are time multiplexed on the same line ($\overline{SKP}/\overline{INT}$). Since the HM-6100 samples skip and interrupt data at separate times there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits (IE1-4) when LXMAR is high. Interrupt requests are asserted by the PIE driving the $\overline{INT}/\overline{SKP}$ line low. During IOTA of SKIP instructions the $\overline{INT}/\overline{SKP}$ reflects the SENSE FF data when $\overline{DEVSEL}$ is low and XTC is high. If the SENSE flip flop is set, the $\overline{INT}/\overline{SKP}$ line is driven low to cause the HM-6100 to skip the next instruction. All these outputs are open drain.

CONTROL LINES				OPERATION	DESCRIPTION
$\overline{SKP}$	$\overline{C0}$*	$\overline{C1}$	$\overline{C2}$		
H	H	H	H	PIE ← AC	The contents of the AC is sent to the PIE.
H	H	L	H	AC ← AC V PIE	Data is received from the PIE, OR'ed with the data in the AC and the result stored in the AC.
H	H	L	L	PC ← Vector Address	Vector address received from PIE and loaded into PC. This is referred to as an absolute jump.
L	H	H	H	PC ← PC + 1	Forces Microprocessor to skip next sequential instruction.

NOTE: *The $\overline{C0}$ line must be connected to V_{CC} using a pull-up resistor.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the HM-6100 via the RCRA and WCRA commands.

The format and meaning of control bits are shown below.

FL (1-4) – Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits under software control changes the corresponding FLAG outputs.

IE (1-4) – A high level on INTERRUPT ENABLE enables interrupts for the SENSE inputs.

Otherwise these inputs provide conditional skip testing as defined by the SKIP1-4 instructions.

WP (1-2) – A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs.

0	1	2	3	4	5	6	7	8	9	10	11
FL4	FL3	FL2	FL1	WP2	*	WP1	*	IE4	IE3	IE2	IE1

* = Don't Care

CONTROL REGISTER B (CRB)

The CRB can be written by the HM-6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown.

SL (1-4) – A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level in the SL bits causes the SENSE inputs to be edge sensitive. An interrupt request is generated only if a sense line is set up to be edge sensitive and interrupts are enabled via the IE bits of CRA.

SP (1-4) – A high level on the SENSE POLARITY bits causes the flip flop to be set by high level or positive going edge. A low level causes the flip flop to be set by a low level or negative going edge.

0	1	2	3	4	5	6	7	8	9	10	11
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1	*	*	*	*

* = Don't Care

VECTOR REGISTER

A hardware priority network uniquely selects a PIE to provide a vectored address. The first IOT command of any type, after the HM-6100 signal INTERRUPT GRANT goes high, resets the INTGNT line to a low level. The INTGNT signal is used to freeze the priority network and enable vector generation. The highest priority PIE has PIN tied to V_{CC}. The lowest priority PIE is the last one on the chain. Within the PIE, SENSE1 has the highest priority and SENSE 4 has the lowest. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt. If PIN is tied to GND, then the PIE will respond as a non-vectored interrupt device.

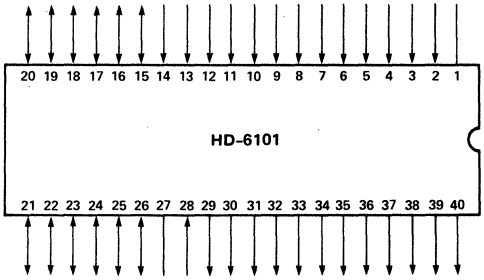
0	1	2	3	4	5	6	7	8	9	10	11
VECTOR REGISTER										VPRI	

VPRI	CONDITIONS
00	SENSE 1
01	SENSE 2
10	SENSE 3
11	SENSE 4

Pin Definitions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	V_{CC}		Positive voltage
2	INTGNT	H	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	H	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	PROG	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the sense flip flop to be set by a level while a low SL level causes then sense flip flop to be set by an edge. A high SP level will cause the sense flip flop to be set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the sense flip flop is set by an edge.
5	SENSE 3	PROG	See pin 4 – SENSE 4
6	SENSE 2	PROG	See pin 4 – SENSE 4
7	SENSE 1	PROG	See pin 4 – SENSE 4

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
8	SEL 3	TRUE	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.
9	SEL 4	TRUE	See Pin 8 – SEL 3
10	LXMAR	H	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	TRUE	See Pin 8 – SEL 3
12	SEL 6	TRUE	See Pin 8 – SEL 3
13	XTC	H	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on $\overline{DEVSEL}$ initiates a "read" operation. When XTC is low, a low going pulse on $\overline{DEVSEL}$ initiates a write operation.
14	SEL 7	TRUE	See Pin 8 – SEL 3
15	DX 0	TRUE	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	TRUE	See Pin 15 – DX 0
17	DX 2	TRUE	See Pin 15 – DX 0
18	DX 3	TRUE	See Pin 15 – DX 0
19	DX 4	TRUE	See Pin 15 – DX 0
20	DX 5	TRUE	See Pin 15 – DX 0



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX 6	TRUE	See Pin 15 – DX 0
22	DX 7	TRUE	See Pin 15 – DX 0
23	DX 8	TRUE	See Pin 15 – DX 0
24	DX 9	TRUE	See Pin 15 – DX 0
25	DX 10	TRUE	See Pin 15 – DX 0
26	DX 11	TRUE	See Pin 15 – DX 0
27	GND		
28	$\overline{DEVSEL}$	L	The $\overline{DEVSEL}$ input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	PROG	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	PROG	See Pin 29 – FLAG 4
31	FLAG 2	PROG	See Pin 29 – FLAG 4
32	FLAG 1	PROG	See Pin 29 – FLAG 4
33	$\overline{C1}$	L	The PIE decodes address, control and priority information and asserts outputs $\overline{C1}$ and $\overline{C2}$ during the IOTA cycle to control the type of data transfer. These outputs are open drain for bussing and require a pullup register to V_{CC}. $\overline{C1}$(L), $\overline{C2}$(L) - vectored interrupt $\overline{C1}$(L), $\overline{C2}$(H) - $\overline{READ1}$, $\overline{READ2}$ or RRA commands $\overline{C1}$(H), $\overline{C2}$(H) - all other instructions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
34	$\overline{C2}$	L	See Pin 33 – $\overline{C1}$
35	$\overline{READ1}$	PROG	Outputs $\overline{READ1}$ and $\overline{READ2}$ are used to gate data from peripheral devices onto the DX bus for input to the **HM-6100** Note the data does not pass through the PIE.
36	WRITE1	PROG	Outputs WRITE1 and WRITE2 are used to gate data from the **HM-6100** DX bus into peripheral devices. Data does not pass through the PIE.
37	$\overline{READ2}$	PROG	See Pin 35 – $\overline{READ1}$
38	WRITE2	PROG	See Pin 36 – WRITE1
39	$\overline{SKP/INT}$	L	The PIE asserts this line low to generate interrupt requests and to signal the **HM-6100** when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	H	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PIN input of the next lower priority PIE in the chain.